

FIG. 1

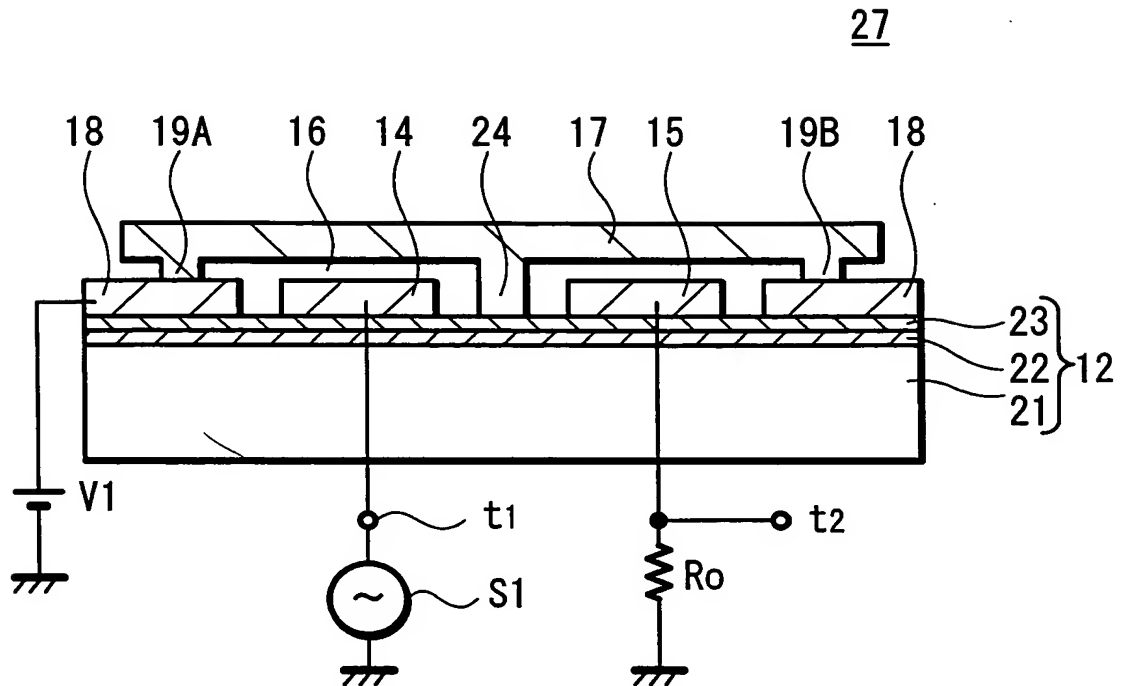


FIG. 2

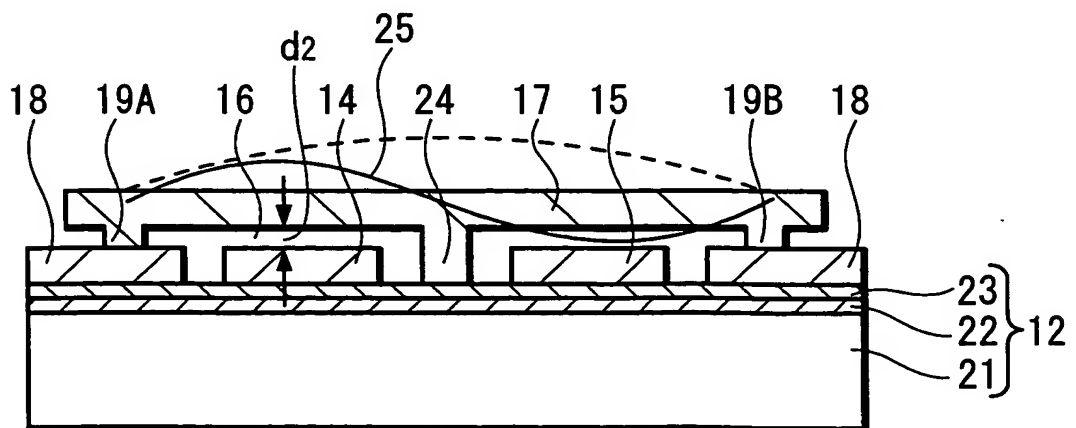


FIG. 3A

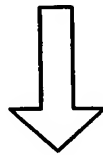
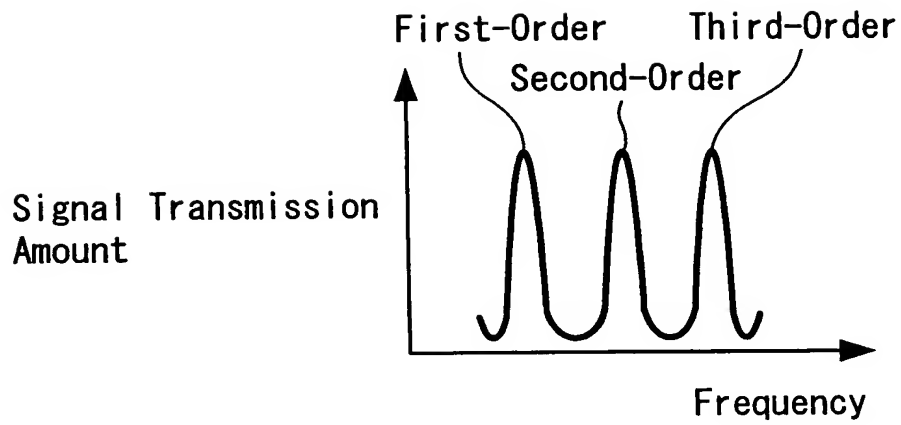


FIG. 3B

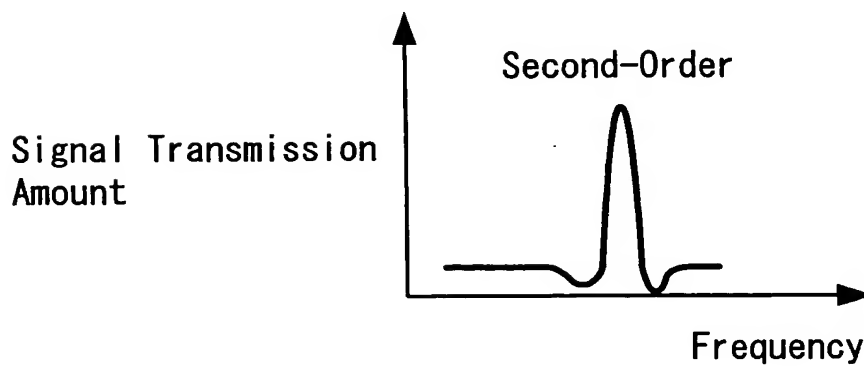


FIG. 4

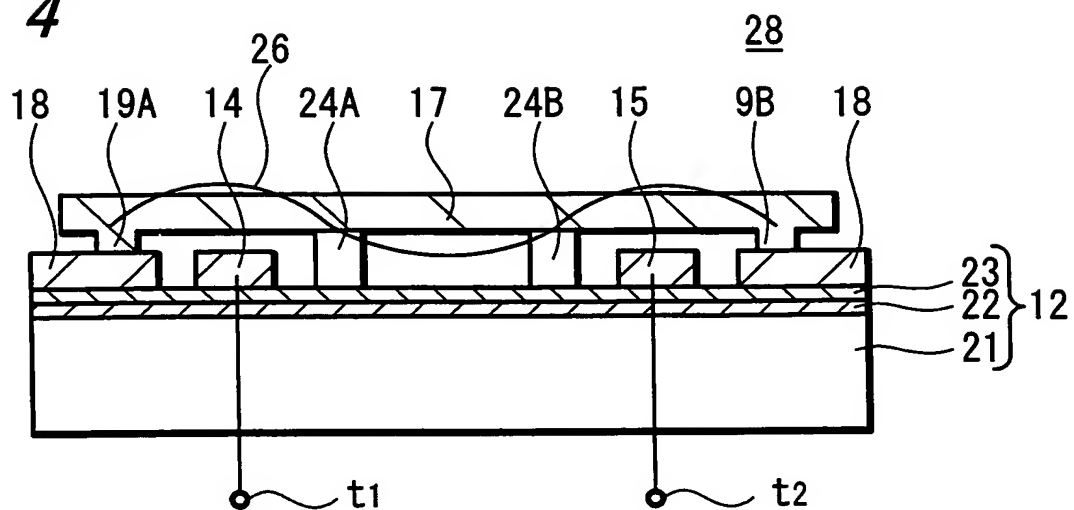


FIG. 5

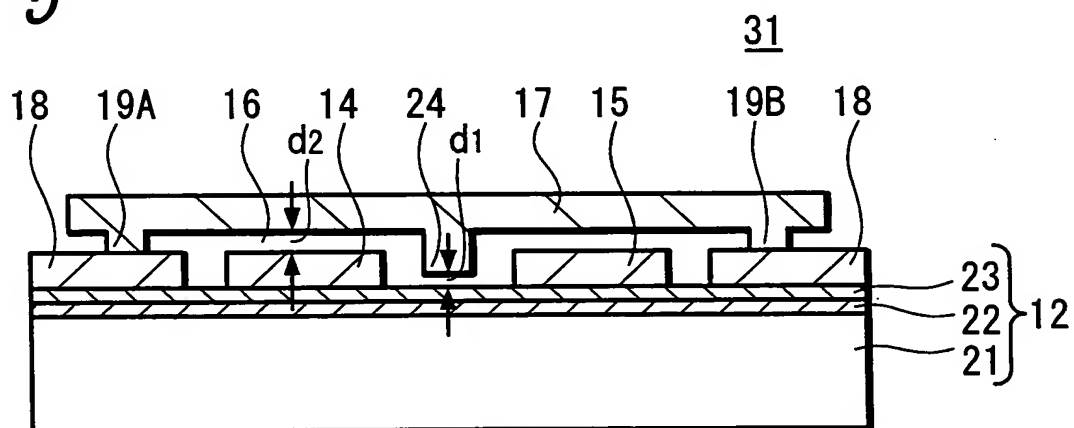


FIG. 6

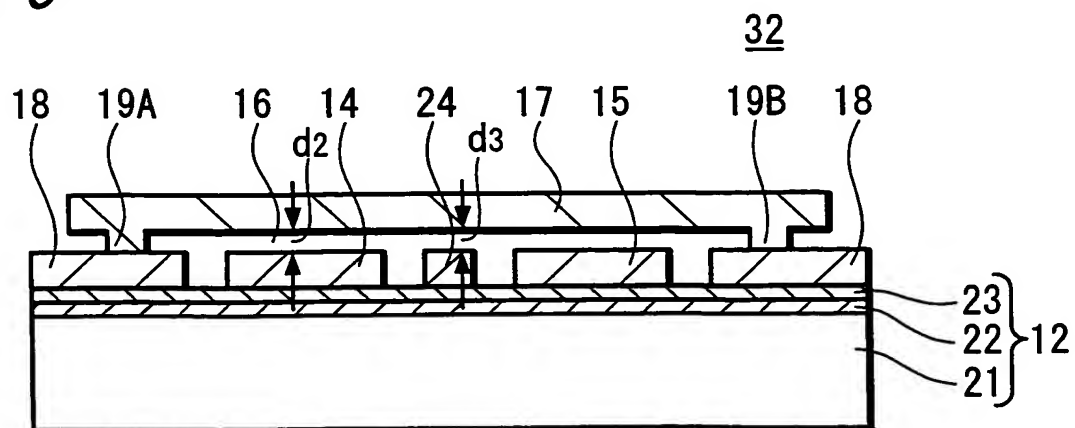


FIG. 7A

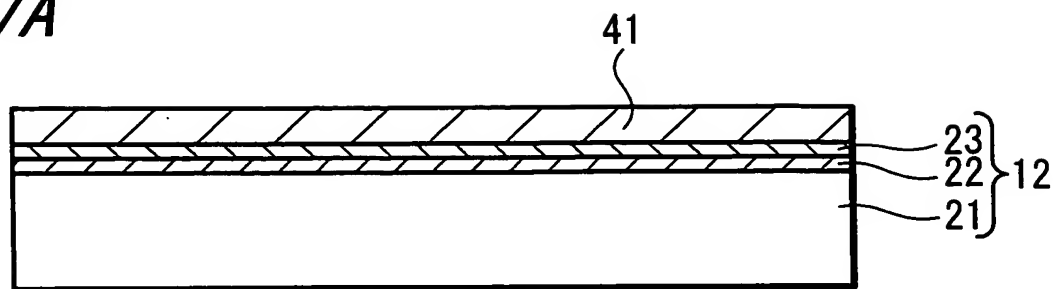


FIG. 7B

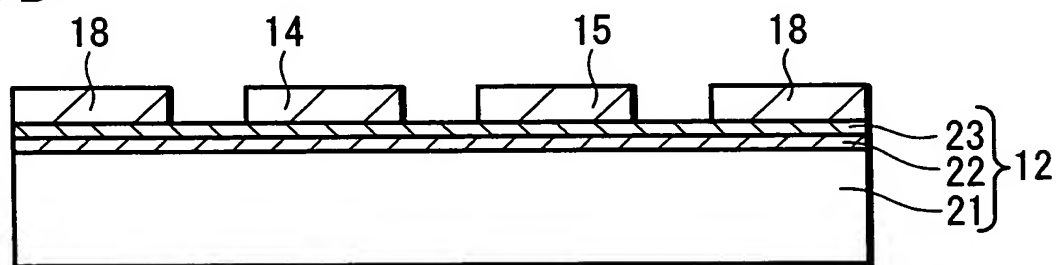


FIG. 7C

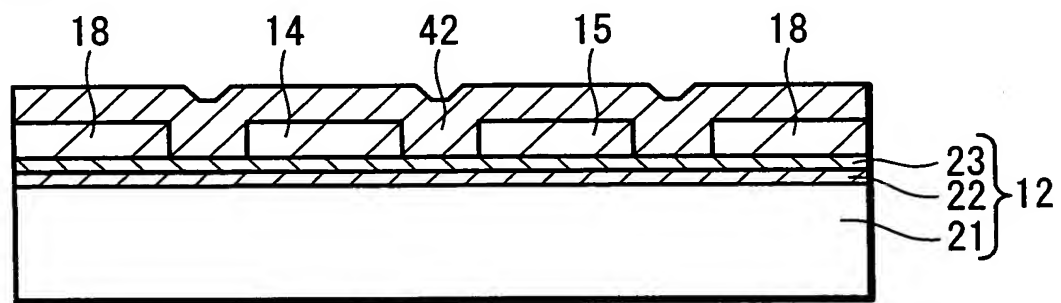


FIG. 7D

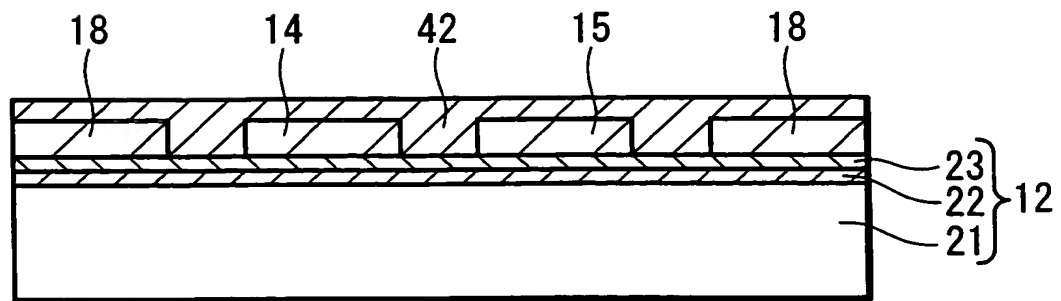


FIG. 8A

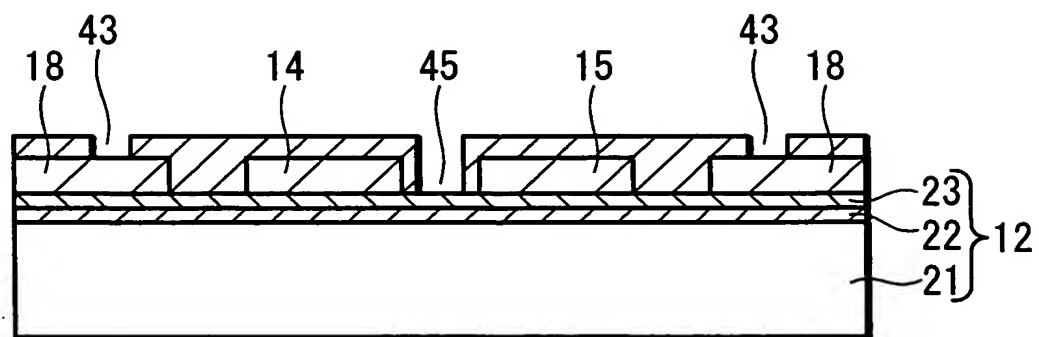


FIG. 8B

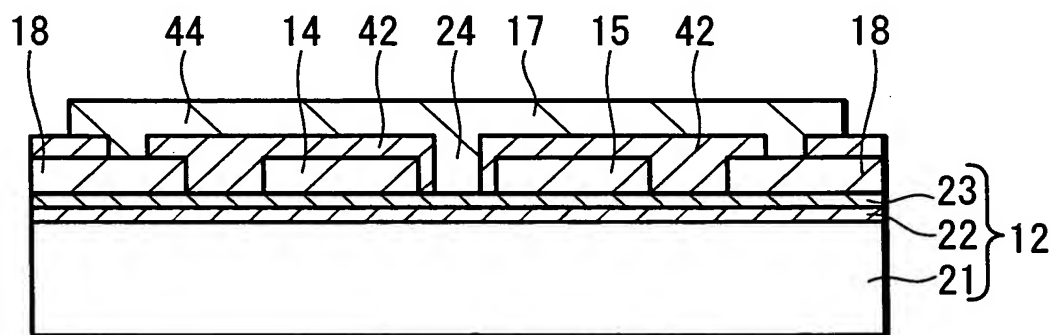


FIG. 8C

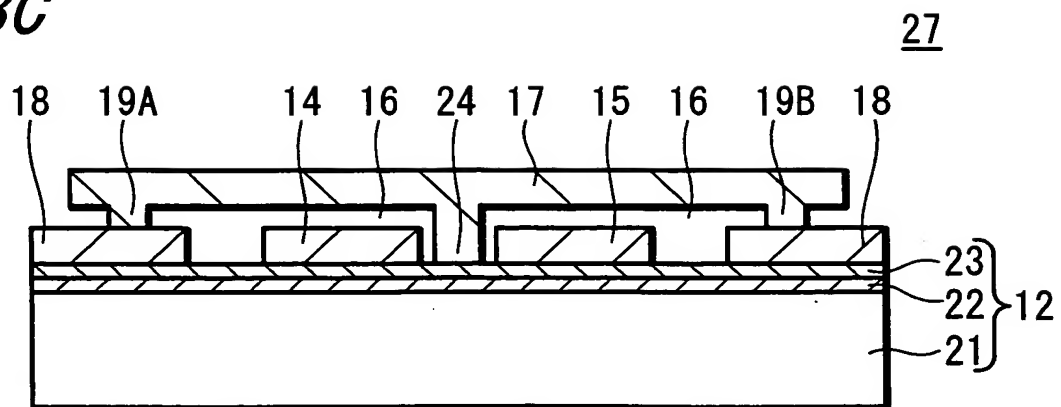


FIG. 9A

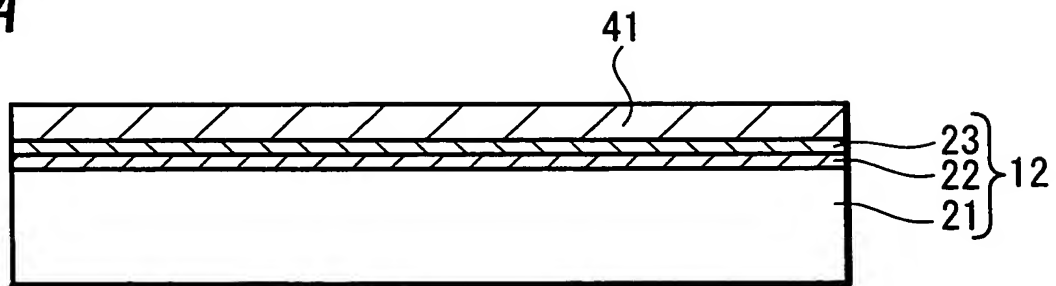


FIG. 9B

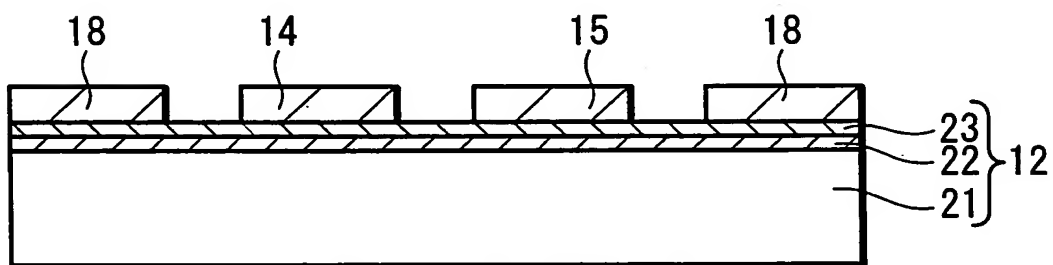


FIG. 9C

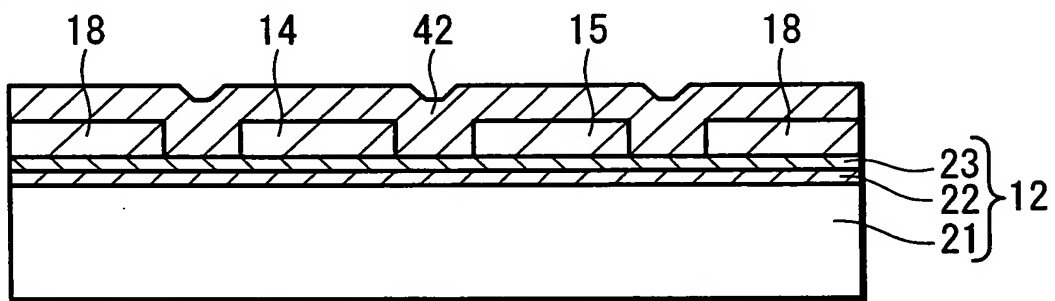


FIG. 9D

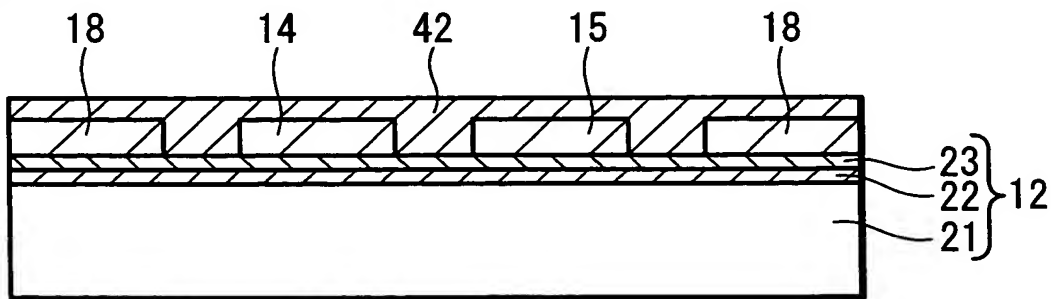


FIG. 10A

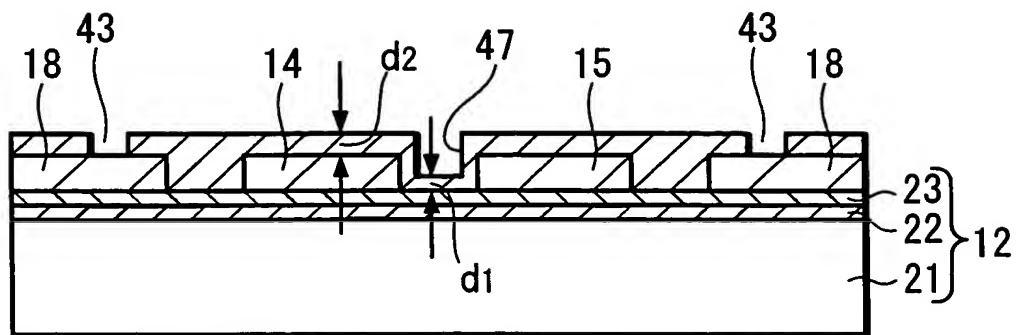


FIG. 10B

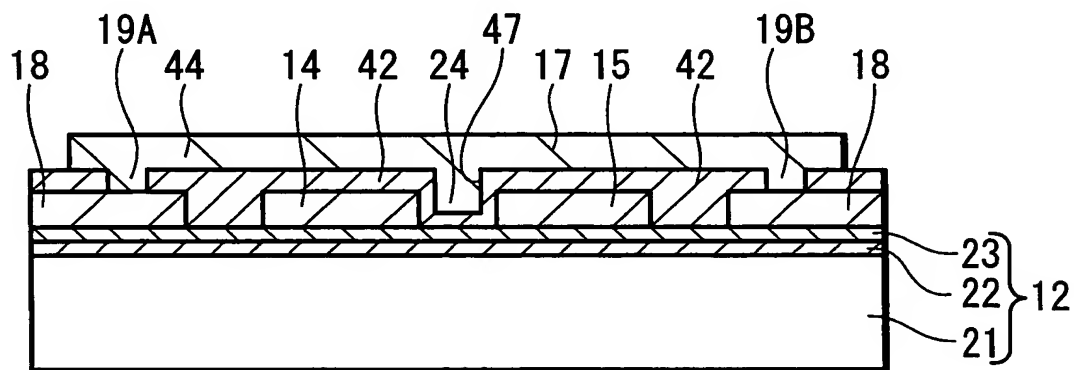


FIG. 10C

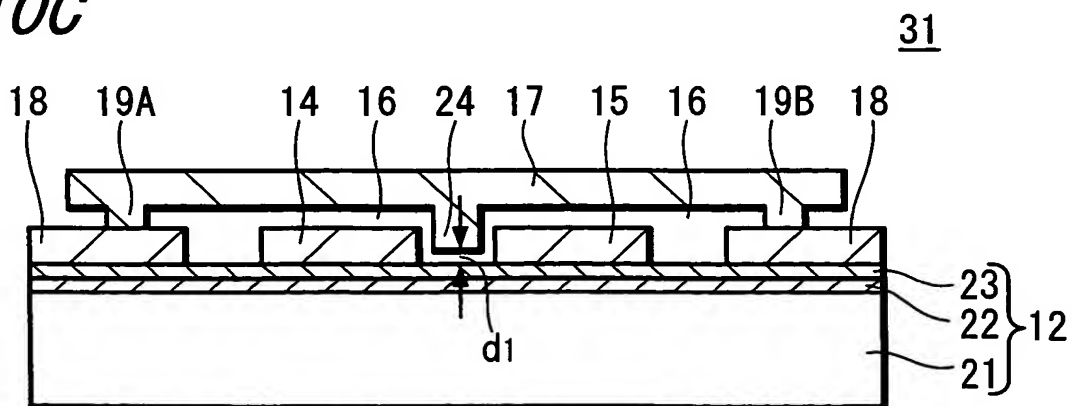


FIG. 11A

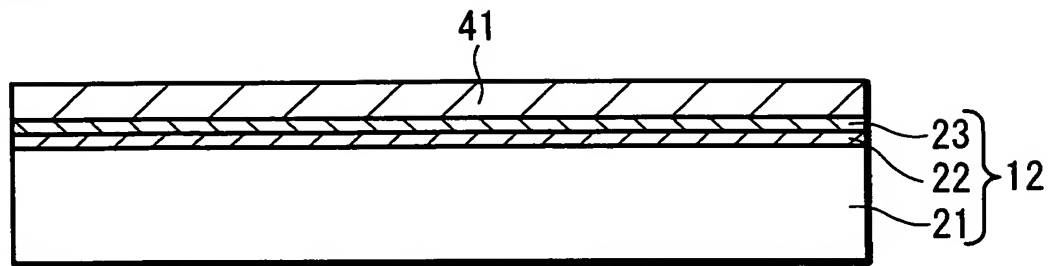


FIG. 11B

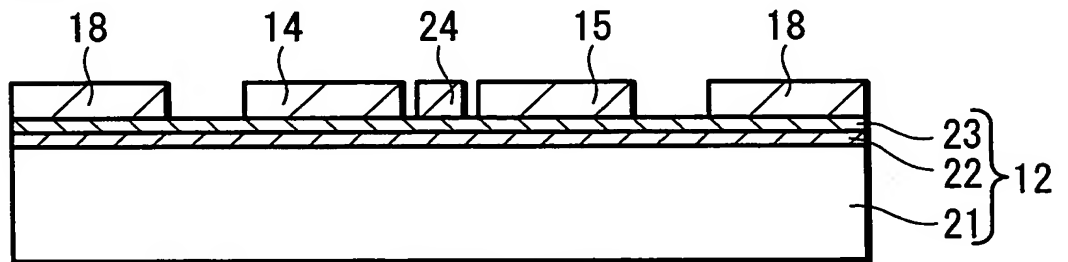


FIG. 11C

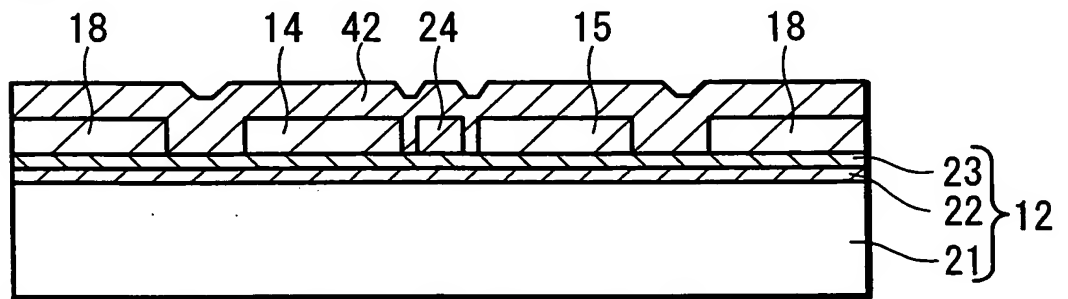


FIG. 11D

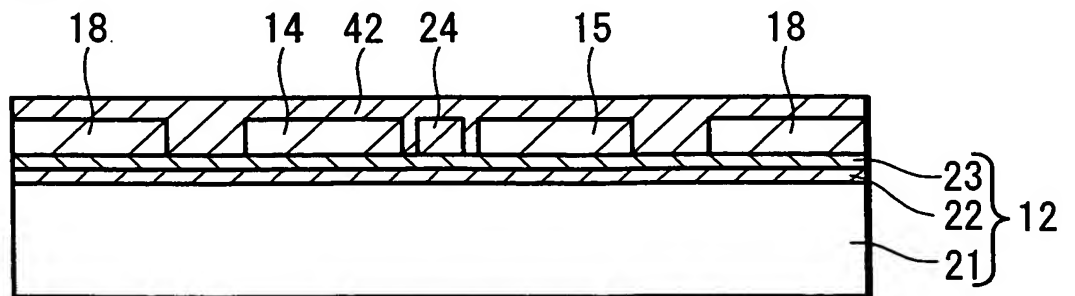


FIG. 12A

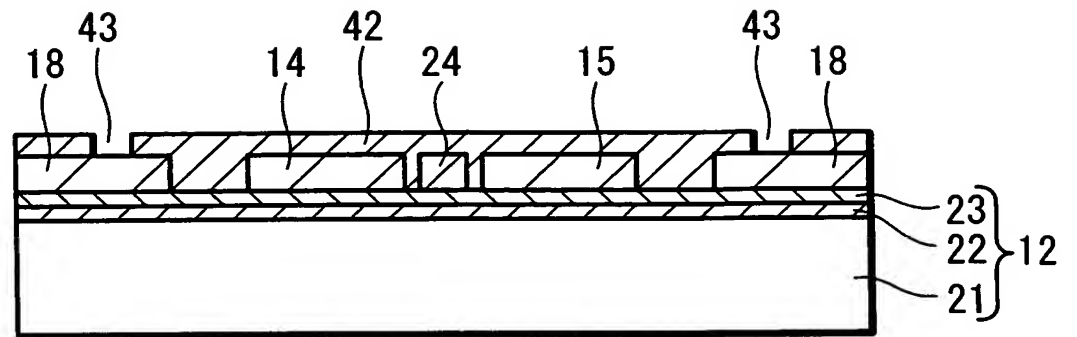


FIG. 12B

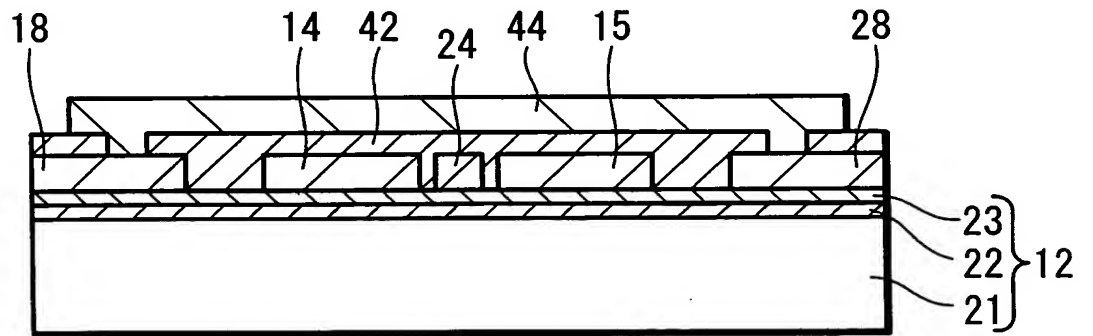


FIG. 12C

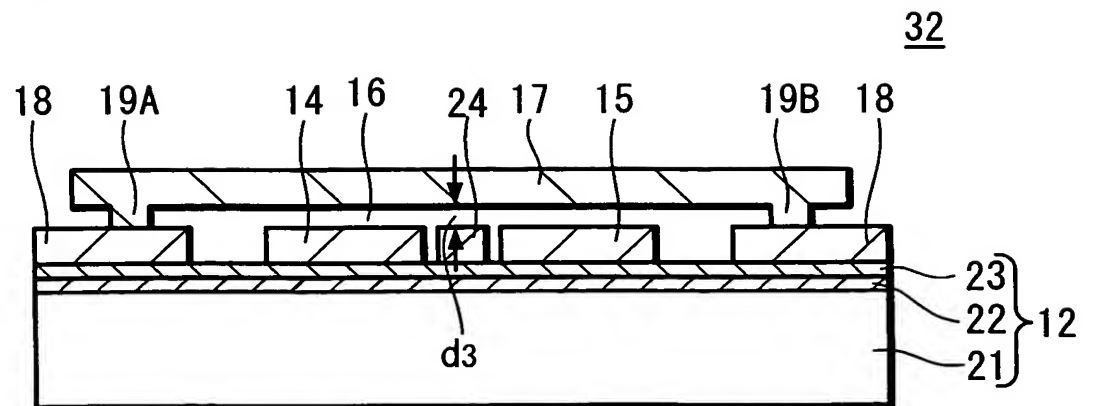


FIG. 13

The diagram illustrates a receiver system architecture. An antenna (207) is connected to a filter (206) and a switch (205). The signal path then splits into two main branches: a baseband processing branch (240) and a transmission PLL branch (203). The baseband processing branch (240) includes a Channel Selection PLL (251) and an AGC (233) block. The signal is processed through a series of filters (222, 232) and mixers (221, 223, 224, 225) before being converted to I and Q components (254I, 254Q) by ADCs (253I, 253Q). The transmission PLL branch (203) includes a Transmission PLL (203) and a series of filters (206, 207) and mixers (201, 202, 203, 204) before being converted to I and Q components (201I, 201Q) by DACs (202I, 202Q). The system also includes an IF PLL (252) and a 90-degree phase shifter (243) to provide phase-shifted signals to the mixers.

FIG. 14

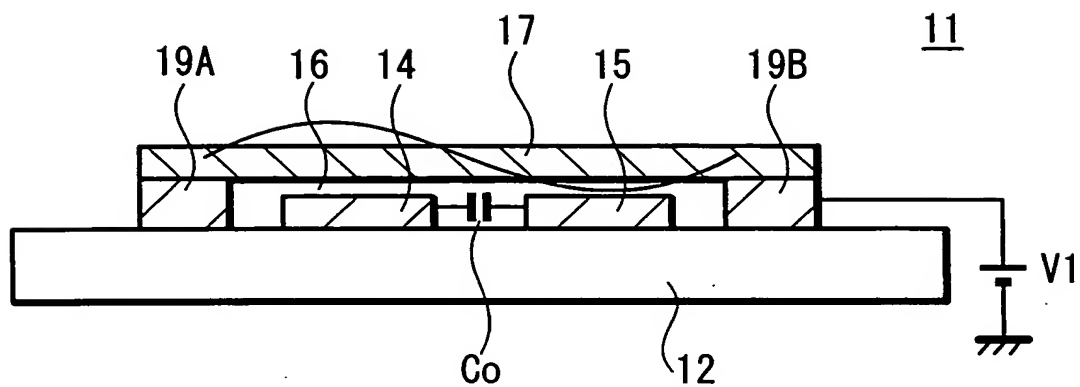
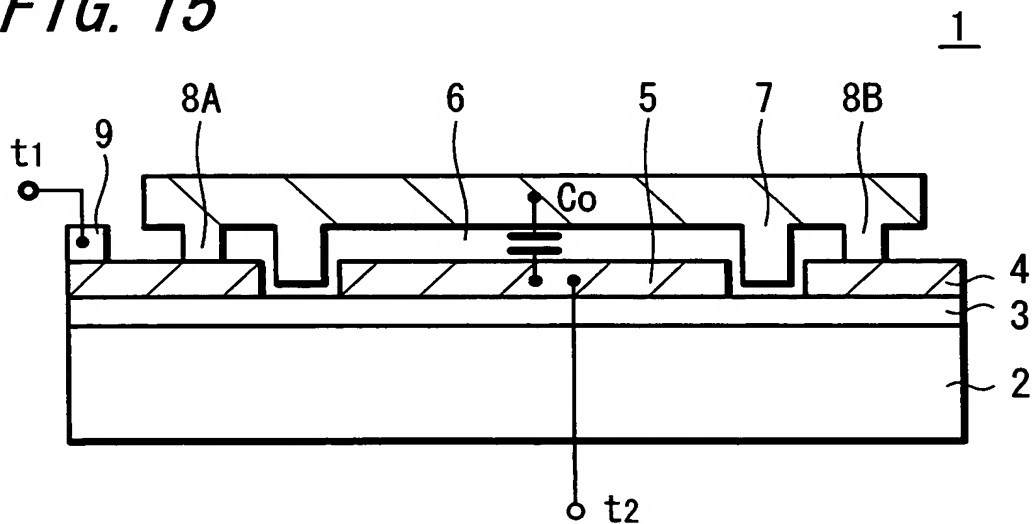


FIG. 15



DESCRIPTION OF REFERENCE NUMERALS

1 --- OSCILLATION ELEMENT
2 --- SEMICONDUCTOR SUBSTRATE
3 --- INSULATION FILM
4 --- INPUT-SIDE WIRING LAYER
11, 27, 28, 31, 32 --- MEMS-TYPE RESONATOR
12 --- SUBSTRATE
14, **14A, 14B** --- INPUT ELECTRODE
5, 15 --- OUTPUT ELECTRODE
6, 16 --- SPACE
7, 17 --- OSCILLATION ELECTRODE
18 --- WIRING LAYER
8 [8A, 8B], 19 [19A, 19B] --- SUPPORT PORTION
21 --- SILICON SUBSTRATE
22 --- SILICON OXIDE FILM
23 --- SILICON NITRIDE FILM
24 [24A, 24B] --- SUPPORT COLUMN
25 --- SECOND-ORDER OSCILLATION MODE
26 --- THIRD-ORDER OSCILLATION MODE
41 --- CONDUCTIVE FILM
42 --- SACRIFICE LAYER
43 --- CONTACT HOLE
44 --- CONDUCTIVE FILM
45, 47 --- OPENING
31 --- SILICON NITRIDE FILM

32 --- SILICON NITRIDE FILM
 33 --- INSULATION FILM
 34 --- SILICON SUBSTRATE
 S1 --- HIGH FREQUENCY SIGNAL
 t1 --- INPUT TERMINAL
 t2 --- OUTPUT TERMINAL
 V1 --- DC BIAS VOLTAGE
 36 --- POLYCRYSTALLINE SILICON FILM
 37 --- SILICON OXIDE FILM
 38 --- OPENING
 39 --- SACRIFICE LAYER
 41 [41A, 41B] --- OPENING
 42 --- CONDUCTIVE MATERIAL LAYER
 201I, 201Q --- DIGITAL/ANALOGUE CONVERTER
 202I, 202Q, 211I, 211Q --- BAND-PASS FILTER
 210 --- MODULATOR
 212I, 212Q --- MIXER
 203 --- PLL CIRCUIT
 213 --- PHASE SHIFTER
 214 --- ADDER
 215 --- BUFFER AMPLIFIER
 204 --- POWER AMPLIFIER
 205 --- TRANSMISSION-RECEPTION SWITCHING UNIT
 206 --- HIGH FREQUENCY FILTER
 207 --- ANTENNA

220 --- HIGH FREQUENCY PORTION
221 --- LOW NOISE AMPLIFIER
244I, 244Q --- BUFFER AMPLIFIER
222, 232 --- BAND-PASS FILTER
223, 225, 231, 234 --- BUFFER AMPLIFIER
224 --- MIXER
251 --- CHANNEL SELECTION PLL CIRCUIT
233 --- AGC CIRCUIT
240 --- DEMODULATOR
252 --- INTERMEDIATE FREQUENCY PLL CIRCUIT
242I --- MIXER
243 --- PHASE SHIFTER
253I, 253Q --- BAND-PASS FILTER
254I, 254Q --- ANALOGUE/DIGITAL CONVERTER